Digital Control of Isolated Two-Stage DC-DC Converter with Synchronization Considered

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Abstract—The green energy transfer with isolation is used to transfer the energy which can not be used directly to the energy which can be utilized directly. This is achieved via switching control, i.e. duty-cycle control. However, by this way, the low-duty cycle is likely to deteriorate the utilization effectiveness of semiconductor devices and magnetic components. Consequently, to conquer this problem, a novel control topology is proposed herein and applied to a two-stage isolated voltage-boosting DC-DC converter with synchronization of gate driving signals considered, along with some simulated and experimental results provided to demonstrate its feasibility.

Index Terms—Green energy, switching control, duty-cycle control, utilization effectiveness, semiconductor device, magnetic component.

I. INTRODUCTION

As generally recognized, recently, the green energy [1-6], created from the wind, the photovoltaic, the fuel cell, the biomass, the tide wave, the geothermal, etc., is attracted by people due to shortage of the petroleum and increase in the environmental pollution. However, the output of the green power is unstable and can not be used directly, which requires energy transfer based on switching control to get stable and usable energy. In general, the isolated converter topology is single-stage, such as the half-bridge converter [7-9], full-bridge converter [10-14], push-pull converter [15], multi-stage cascaded converter [16-19], etc. These converters are controlled by duty cycles to boost and stabilize output voltages. However, if these converters operate on the condition of low-duty cycles, then semiconductor devices and magnetic components can not be employed under the maximum utilization effectiveness. Consequently, in this paper, a new control topology is presented, which cascades two different types of converters. The first stage is the boost converter with small output capacitance and the second stage is the push-pull converter with relatively small output inductance. The output voltage of the second stage is sensed and fed back to the controller of the first stage such that the output voltage of the second stage is kept constant at the desired value, whereas the second stage takes a major role of voltage boosting. To explain clearly, the first stage, the boost converter, is in charge of stabilization of the output voltage and the second stage, the push-pull converter, is responsible for not only isolation and but voltage boosting under the maximum duty cycle so as to achieve the maximum fixed utilization effectiveness of the semiconductor devices and magnetic components [20] of the push-pull converter.

On the other hand, the digital signal processor (DSP) control [21-27] is getting more and more attracted in the world, because some difficult processes can be easily realized based on the DSP. Thus, the DSP is utilized herein to synchronously trigger the main switches of two stages to reduce the output ripple and to increase the stability of the system, to be described later. In this paper, some simulated and experimental results are provided to demonstrate its effectiveness.

II. PROPOSED SYSTEM CONFIGURATION

In Fig. 1, the proposed two-stage converter contains the first stage, boost converter, cascaded with the second stage, push-pull converter. The main power stage of the boost converter is composed of one inductor Lb, one MOSFET switch Sb, one diode Db and one capacitorCb, whereas the main power stage of the push-pull converter consists of two MOSFET switches Sp1 and Sp2, one transformerTp, two rectification diodesDp1 andDp2, one capacitor Cp. Besides, the sensed signal, sent to the digital control board, contains the output voltage of the push-pull converter. As for the digital control board, it includes the analog-to-digital converter (ADC), the control kernel based on TMS320F2812 and the pulse width modulation (PWM) generator. Besides, M1, M2, and M3 are PWM signals for S1, S2, and S3, respectively.

![Fig. 1. Proposed system configuration.](image)

III. PROPOSED CONTROL STRATEGY

In Fig. 1, the first stage is the boost converter and the second stage is the push-pull converter. The major features of the proposed control for this two-stage converter are described in detail as follows. The output voltage of the second stage is sensed and fed back to the first stage such that the output
voltage of the second stage is stabilized due to the first stage controlling the input voltage of the second stage, which is also the output voltage of the first stage. And on the other hand, the second stage plays a role of voltage boosting as well as isolation under the maximum fixed duty cycle so as to obtain the maximum utilization effectiveness of the semiconductor devices and magnetic components of the push-pull converter.

As generally known, basic operating principles of the boost converter and the push-pull converter are easy to understand and hence are not described herein. As for the push-pull converter, its voltage stresses on two switches of the push-pull converter are at least two times of its input voltage. Therefore, the push-pull converter is not suitable for the high-voltage input. Besides, the central tape is taken at the primary, thereby only half of the windings at the primary participate in energy transfer during the half of switching period. Since the output voltage of the two-stage converter, which is also the output voltage of the push-pull converter, is sensed and sent to the controller of the boost converter, the small-capacitance output voltage of the boost converter, which is also the input voltage of the push-pull converter, is varied so as to keep the output voltage of the two-stage converter as constant as possible at the prescribed DC value, under the fixed duty cycle of 0.48 for the push-pull converter. Also, since the dead time between two switches of the push-pull converter, determined by the required delay time of the MOSFET switch, is very small, the output inductance of the push-pull converter is essentially small or even zero, and hence the output voltage ripple is very small.

![Fig. 2. PSIM-based system circuit.](image)

IV. SIMULATION AND EXPERIMENTAL RESULTS

Before this section is discussed, there are some specifications to be described as follows: (i) input DC voltage range is between 37.8V and 46.2V with rated input voltage of 42V; (ii) output DC voltage is 200V; (iii) rated output power is 300W; (iv) switching frequencies for the boost converter and the push-pull converter are 100kHz and 50kHz, respectively; (v) four 220μF aluminum electrolytic capacitors paralleled are chosen for the input capacitor of the boost converter; (vi) one 22μF MPP capacitor is selected for the output capacitor of the boost converter; (vii) one 220μF aluminum electrolytic capacitor is chosen for the output capacitor of the push-pull converter; (viii) value of the input inductor Lp of the boost converter is actually set to 100μH whereas there is no output inductor for the push-pull converter; and (ix) boost converter operates in CCM under rated conditions.

Figs. 3 to 5 show the simulated results based on PSIM at rated input voltage of 42V under rated load on condition that $M_2$ and $M_3$ are synchronized with $M_1$ at the rising edge of $M_1$, in the middle of the turn-on period of $M_1$, and at the falling edge of $M_1$, respectively. And Figs. 6 to 8 display the corresponding simulated voltage ripples of the boost converter, whereas Figs. 9 to 11 depict the simulated voltage ripples of the push pull converter for these three cases. It is noted that the voltage ripple in case 1 is the smallest among three cases for the boost converter to be considered whereas the result is the same for the push pull converter to be considered.

On the other hand, Figs. 12 to 24 display the measured results for the three cases mentioned above. Fig. 12 shows the dead time between PWM signals $M_2$ and $M_3$ for the push pull converter. Figs. 13 to 15 illustrate relationships between $M_1$ and $M_3$ for these three cases. Figs. 16 to 18 show waveforms relevant to $M_1$, the output voltage of the boost converter, and the output voltage of the push pull converter. It is obvious that the output voltage of this two-stage converter can be stabilized at the desired value for any case, and the trend of voltage ripples of the boost converter for these three cases is the same as that in simulation. Figs. 19 to 21 describe output ripples of the push pull converter for these three cases. It is evident that the corresponding trend is the same as that in simulation, also. Besides, Figs. 22 to 24 show relevant waveforms at rated input voltage of 42V under rated load on condition that $M_2$ and $M_1$ are non-synchronized with $M_1$. It can be seen that the system approaches divergence. Based on the mention above, this converter operates in case 1 has the best performance among all cases.

![Fig. 3. $M_2$ and $M_3$ are synchronized with $M_1$ at the rising edge of $M_1$.](image)
Fig. 4. \(M_2\) and \(M_3\) are synchronized with \(M_1\) in the middle of the turn-on period of \(M_1\).

Fig. 5. \(M_2\) and \(M_3\) synchronized with \(M_1\) at the falling edge of \(M_1\).

Fig. 6. Simulated voltage ripple of \(V_b\) at input voltage of 42V under the rated load on condition that \(M_2\) and \(M_3\) are synchronized with \(M_1\) at the rising edge of \(M_1\).

Fig. 7. Simulated voltage ripple of \(V_b\) at input voltage of 42V under rated load on condition that \(M_2\) and \(M_3\) are synchronized with \(M_1\) in the middle of the turn-on period of \(M_1\).

Fig. 8. Simulated voltage ripple of \(V_b\) at input voltage of 42V under rated load on condition that \(M_2\) and \(M_3\) are synchronized with \(M_1\) at the falling edge of \(M_1\).

Fig. 9. Simulated voltage ripple of \(V_o\) at input voltage of 42V under rated load on condition that \(M_2\) and \(M_3\) are synchronized with \(M_1\) at the rising edge of \(M_1\).

Fig. 10. Simulated output voltage ripple of \(V_o\) at input voltage of 42V under rated load on condition that \(M_2\) and \(M_3\) are synchronized with \(M_1\) in the middle of the turn-on period of \(M_1\).

Fig. 11. Simulated voltage ripple of \(V_o\) at input voltage of 42V under rated load on condition that \(M_2\) and \(M_3\) are synchronized with \(M_1\) at the falling edge of \(M_1\).
Fig. 12. $M_2$ and $M_3$ to drive the push-pull converter.

Fig. 14. $M_2$ synchronized with $M_1$ at the middle of the turn-on period of $M_1$.

Fig. 16. Measured waveforms at input voltage of 42V under the rated load on condition that $M_2$ and $M_3$ are synchronized with $M_1$ at the rising edge of $M_1$: (1) $M_1$; (2) $V_b$; (3) $V_o$.

Fig. 17. Measured waveforms at input voltage of 42V under the rated load on condition that $M_2$ and $M_3$ are synchronized with $M_1$ in the middle of the turn-on period of $M_1$: (1) $M_1$; (2) $V_b$; (3) $V_o$. 
Fig. 18. Measured waveforms at input voltage of 42V under the rated load on condition that $M_2$ and $M_3$ are synchronized with $M_1$ at the falling edge of $M_1$: (1) $M_1$; (2) $V_b$; (3) $V_o$.

Fig. 19. Measured voltage ripple of $V_o$ at input voltage of 42V under the rated load on condition that $M_2$ and $M_3$ are synchronized with $M_1$ at the rising edge of $M_1$.

Fig. 20. Measured voltage ripple of $V_o$ at input voltage of 42V under the rated load on condition that $M_2$ and $M_3$ are synchronized with $M_1$ in the middle of the turn-on period of $M_1$.

Fig. 21. Measured voltage ripple of $V_o$ at input voltage of 42V under the rated load on condition that $M_2$ and $M_3$ are synchronized with $M_1$ at the falling edge of $M_1$.

Fig. 22. $M_2$ non-synchronized with $M_1$.

Fig. 23. Measured waveforms at input voltage of 42V under the rated load on condition that $M_2$ and $M_3$ are non-synchronized with $M_1$: (1) $M_1$; (2) $V_b$; (3) $V_o$. 

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V. CONCLUSION

The proposed control strategy for the isolated two-stage converter is not only suitable for the boost converter cascaded with the push-pull converter but also for the boost converter cascaded with the half-bridge converter or the full-bridge converter, to obtain the maximum utilization effectiveness of the semiconductor devices and magnetic components of the push-pull converter or the half-bridge converter or the full-bridge converter. And by this way the output inductance can be removed so that the system design can be simplified. Above all, the synchronization between PWM signals is discussed in detail so as to reduce the output voltage ripple and to enhance the stability of the system.

REFERENCES