Chapter 9 ARM Processor Cores

Introduction (1)

- An ARM processor core is the engine within a system that fetches ARM instructions from memory and executes them.
- ARM cores are very small, typically occupying just a few square millimeters of chip area.
- The correct choice of processor core is one of the most critical decisions in the specification of a new system.
Introduction (2)

- The principal current ARM processor core products are described
- Offer a choice of cost, complexity and performance points from which the most effective solution can be selected

ARM7TDMI (1)

- The ARM7TDMI is the current low-end ARM core and is widely used across a range of application, most notably in many digital mobile telephones
- TDMI: Thumb Debug Multiplier EmbeddedICE
The origins of the name are as follows:

- The ARM7, a 3 volt compatible rework of the ARM6 32-bit integer core, with:
- The Thumb 16-bit compressed instruction set;
- On-chip Debug support, enabling the processor to halt in response to a debug request;
- An enhanced Multiplier, with higher performance than its predecessors and yielding a full 64-bit result; and
- EmbeddedICE hardware to give on-chip breakpoint and watchpoint support
ARM7TDMI cycle types

<table>
<thead>
<tr>
<th>mreq</th>
<th>seq</th>
<th>Cycle</th>
<th>Use</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>N</td>
<td>Non-sequential memory access</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>S</td>
<td>Sequential memory access</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>I</td>
<td>Internal cycle – bus and memory inactive</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>C</td>
<td>Coprocessor register transfer – memory inactive</td>
</tr>
</tbody>
</table>
### ARM7TDMI Characteristics

<table>
<thead>
<tr>
<th>Process</th>
<th>0.35 um</th>
<th>Transistors</th>
<th>74,209</th>
<th>MIPS</th>
<th>60</th>
</tr>
</thead>
<tbody>
<tr>
<td>Metal layers</td>
<td>3</td>
<td>Core area</td>
<td>2.1 mm²</td>
<td>Power</td>
<td>87 mW</td>
</tr>
<tr>
<td>Vdd</td>
<td>3.3 V</td>
<td>Clock</td>
<td>0 to 66 MHz</td>
<td>MIPS/W</td>
<td>690</td>
</tr>
</tbody>
</table>

### ARM7TDMI for Synthesis (1)

- The standard ARM7TDMI processor core is a ‘hard’ macrocell, which is to say that it is delivered as a piece of physical layout, customized to the appropriate process technology.
- The ARM7TDMI-S is synthesizable version of the ARM7TDMI, delivered as a high-level language module which can be synthesized using any suitable all library in the target technology.
- It is therefore easier to port to a new process technology than is the hard macrocell.
ARM7TDMI for Synthesis

- The synthesis process supports a number of optional variations on the processor core functionality. These include:
  - Omitting the EmbeddedICE all;
  - Replacing the full 64-bit result multiplier with a smaller and simpler multiplier that supports only the ARM multiply instructions that produce 1 32-bit result

ARM7TDMI Applications

- The ARMTDMI processor core has found many applications in systems with simple memory configurations, usually including a few kilobytes of simple on-chip RAM
- Mobile telephone handset
The ARM8 core was developed at ARM Limited from 1993 to 1996.

Supply the demand for an ARM core with a higher performance than was achievable with the ARM7 3-stage pipeline.

It has now been superseded by the ARM9TDMI and ARM10TDMI.

The performance of a processor core can be improved by:
- Increasing the clock rate
- Reducing the CPI (clock cycles per instruction)

**ARM8 Processor Core Organization**

![Diagram of ARM8 processor core organization]
Double-bandwidth Memory

- ARM8 retains a unified memory but exploits the sequential nature of most memory accesses to achieve double-bandwidth from a single memory.
- It assumes that the memory it is connected to can deliver one word in a clock cycle and deliver the next sequential word half a cycle later concurrently with starting the next access.

ARM8 Integer Unit Organization
ARM8 Applications and Silicon

- ARM8 was designed as a general purpose processor core
- One application of the ARM8 core is to build a high-performance CPU such as the ARM810
- The ARM8 core uses 12454 transistors and operates at speeds up to 72MHz on a 0.5µm CMOS process with three metal layers

ARM9TDMI (1)

- The ARM9TDMI core takes the functionality of ARM7TDMI up to a significantly higher performance level
- Support for the Thumb instruction set and an EmbeddedICE module for on-chip debug
- The performance improvement is achieved by adopting a 5-stage pipeline to increase the maximum clock rate and by using separate instruction and data memory ports to allow an improved CPI (Clock Per Instruction)
ARM9TDMI (2)

- EmbeddedICE
- as ARM7TDMI, plus:
  - hardware single-stepping
  - breakpoints on exceptions
- On-chip coprocessor support:
  - for floating-point, DSP, and so on

ARM9TDMI Organization
ARM7TDMI and ARM9TDMI Pipeline Comparisons

ARM7TDMI: Fetch Decode Execute

- instruction fetch
- Thumb decompress
- ARM decode
- reg. read
- reg. shift/ALU
- reg. write

ARM9TDMI: Fetch Decode Execute

- instruction fetch
- Thumb read
- ARM decode
- reg. shift/ALU
- data memory access
- reg. write

ARM9TDMI Characteristics

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<td>0.25 um</td>
<td>110,000</td>
<td>220</td>
<td>150 mW</td>
<td>1500</td>
</tr>
<tr>
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<td>3</td>
<td>Core area</td>
<td>2.1 mm²</td>
<td>Clock</td>
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ARM10TDMI

- Targets multi-media digital consumer applications
  - high-performance hand-held devices (organizers, smart phones)
  - set top boxes
  - sophisticated UI and 2D-/3D-graphics rendering
  - high performance printers
- Vector floating point Copro. (VFP 10) delivering 600 MFLOPS
- Parallel instruction execution

The ARM10TDMI Pipeline